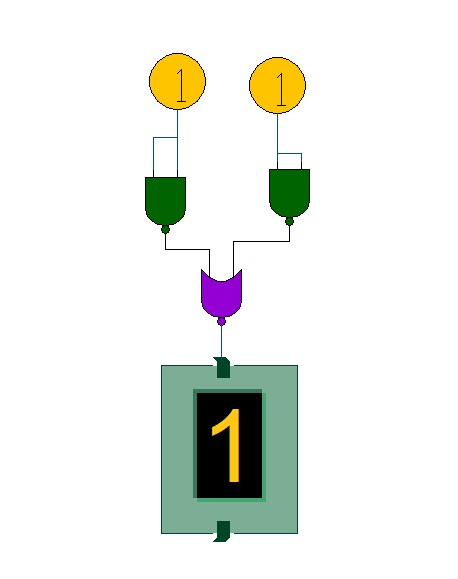
**ASSIGNMENT - 2**

**Q.1 Design AND, OR, and NOT gate using NAND and NOR gate.**

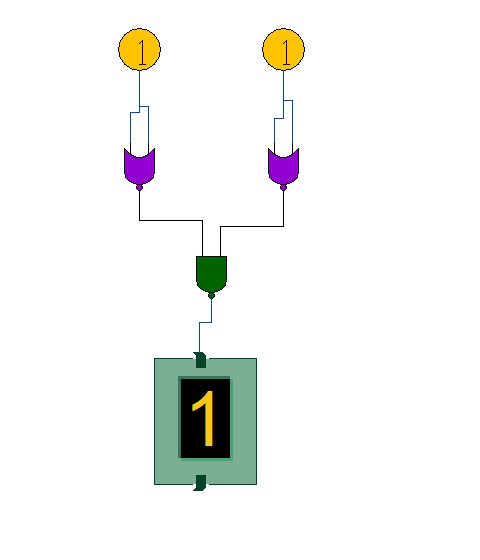
* **AND GATE USING NAND AND NOR GATE**



* **TRUTH TABLE : -**

|  |  |  |
| --- | --- | --- |
| **INPUTS** | | **OUTPUT** |
| **A** | **B** | **AB** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

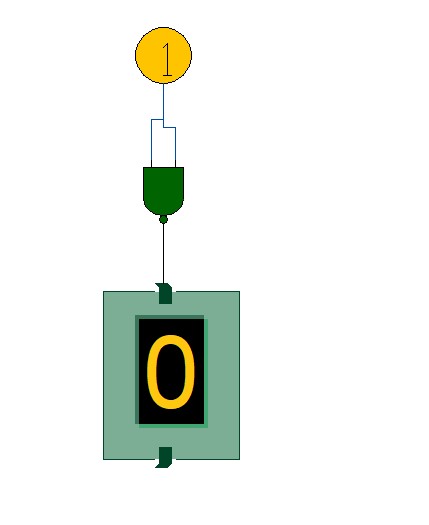
* **OR GATE USING NAND AND NOR GATE.**



* **TRUTH TABLE : -**

|  |  |  |
| --- | --- | --- |
| **INPUTS** | | **OUTPUT** |
| **A** | **B** | **A+B** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **1** |

* **OR GATE USING NAND AND NOR GATE .**

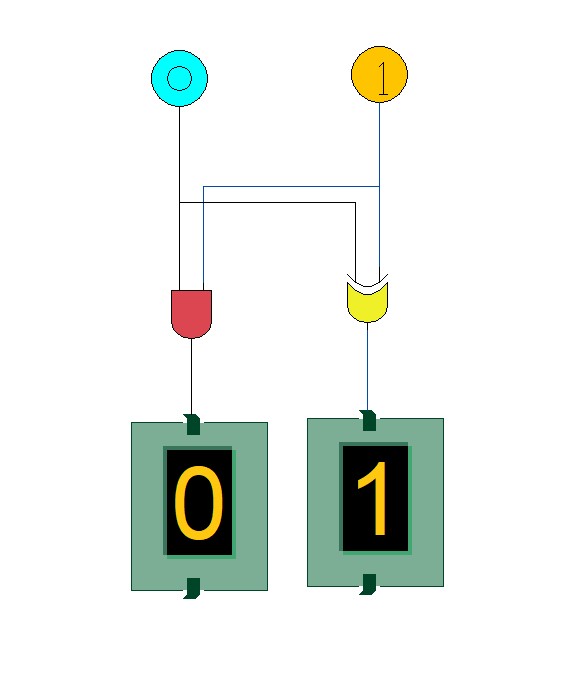


* **TRUTH TABLE : -**

|  |  |
| --- | --- |
| **INPUTS** | **OUTPUT** |
| **A** | **B** |
| **0** | **1** |
| **1** | **0** |

**Q.2 Design a Half Adder and Full adder using basic gates.**

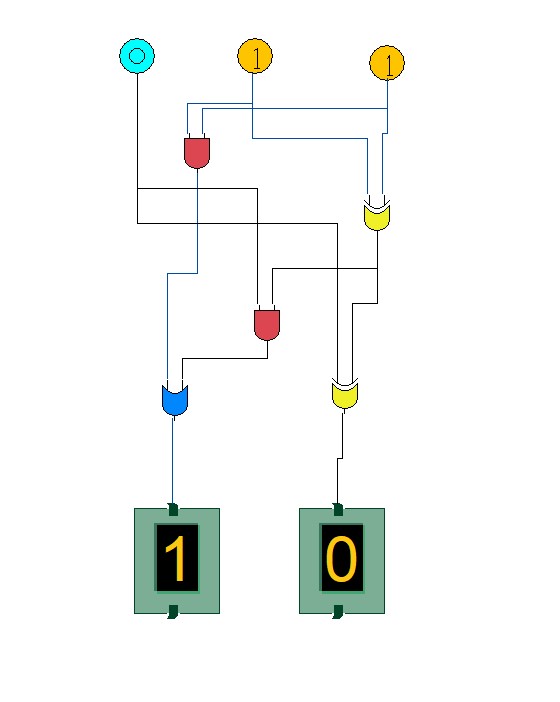
* **Half Adder using Basic gates.**

****

* **TRUTH TABLE : -**

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **SUM** | **CARRY** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |

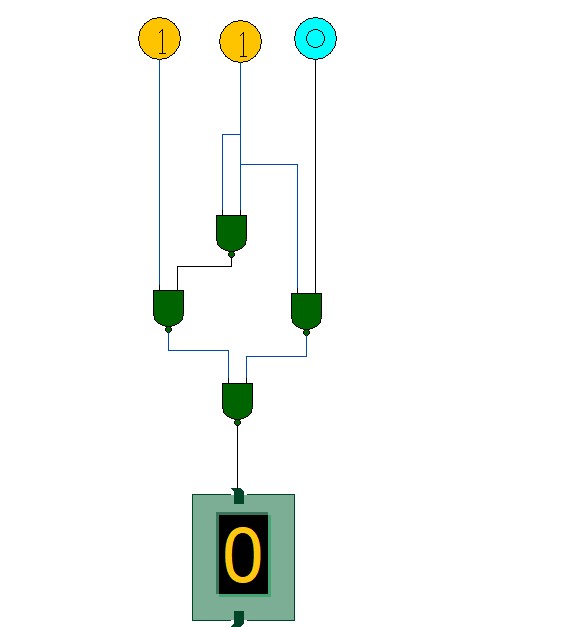
* **FULL ADDER USING BASIC GATES.**

****

* **TRUTH TABLE : -**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **INPUTS** | | | **OUTPUT** | |
| **A** | **B** | **Cin** | **SUM** | **CARRY** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |

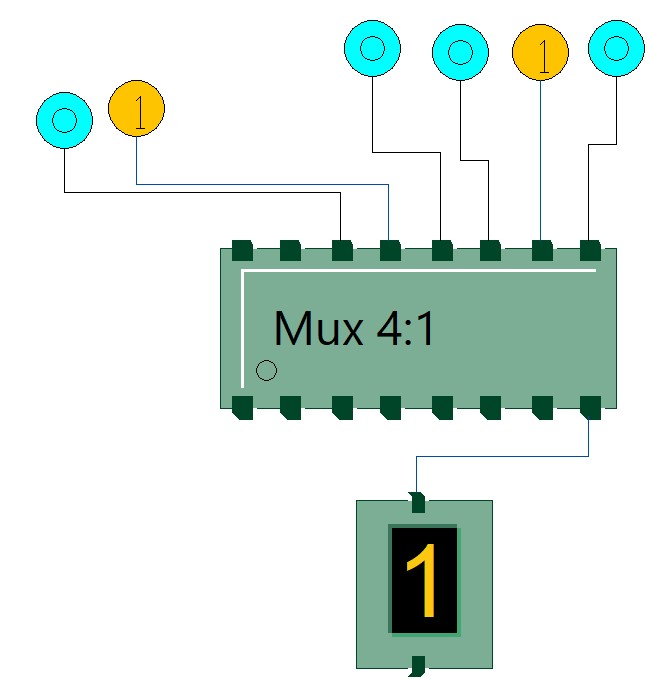
**Q.3 To Design and set up 2:1 Multiplexer(MUX) using only NAND gates.**

****

* **TRUTH TABLE : -**

|  |  |  |  |
| --- | --- | --- | --- |
| **SELECT LINE** | **INPUTS** | | **OUTPUT** |
| **S** | **A** | **B** | **Y** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** |

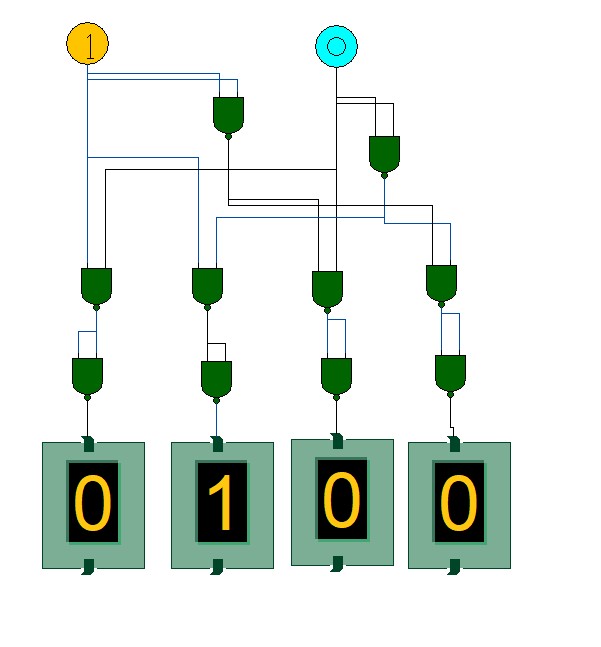
**Q.4 To design and set up 4:1 Multiplexer (MUX) using in the Simulator.**

****

* **TRUTH TABLE : -**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SELECT LINE** | | **OUTPUT** | | | |
| **S1** | **S0** | **Y3** | **Y2** | **Y1** | **Y0** |
| **0** | **0** | **x** | **x** | **x** | **1** |
| **0** | **1** | **x** | **x** | **1** | **x** |
| **1** | **0** | **x** | **1** | **x** | **x** |
| **1** | **1** | **1** | **x** | **x** | **x** |

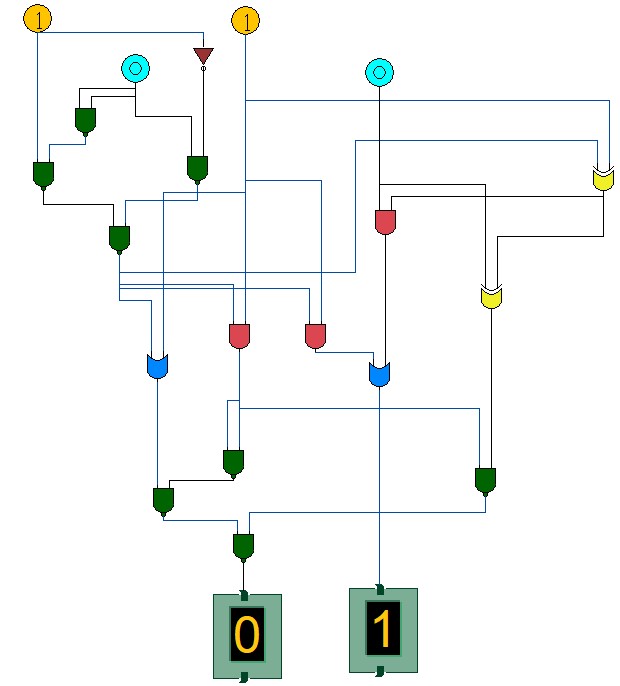
**Q.5 To design and Implement 2 to 4 decoder using NAND gates.**

****

* **TRUTH TABLE : -**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **INPUTS** | | **OUTPUT** | | | |
| **A1** | **A0** | **D3** | **D2** | **D1** | **D0** |
| **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **0** | **1** | **0** | **0** |
| **1** | **1** | **1** | **0** | **0** | **0** |

**Q.6 Design the Arithmetic Logical unit using basic gates.**

****

* **TRUTH TABLE : -**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **F2** | **F1** | **F0** | **ALU Function** | **Carry Out** |

